Total No. of printed pages = 3

CSE 181303

Roll No. of candidate | | | | | | | | | | |

25/2/22 2021

B.Tech. 3rd Semester End-Term Examination

CSE

DIGITAL SYSTEMS

(New Regulation & New Syllabus)

Full Marks – 70 Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer question No. 1 and any *four* from the rest.

1. Choose the correct answer of the following: $(10 \times 1 = 10)$

(i) A ripple counter is a

(a) Synchronous counter (b) Asynchronous counter

(c) Parallel counter (d) None of the above

(ii) The no. of comparators in a 4-bit flash ADC is

(a) 4 (b) 15

(c) 5 (d) 16

(iii) An n-bit ADC using V as reference voltage has a resolution of

(a) $V/2^n$ (b) $V/(2^n-1)$

(c) V.n (d) None of the above

(iv) Which of the following memories must be refreshed many times per second?

(a) EPROM (b) ROM

(c) Static RAM (d) Dynamic RAM

(v) As compared to TTL, ECL has

(a) Lower power dissipation (b) Higher propagation delay

(c) Lower propagation delay (d) Higher noise margin

(vi) The smallest number that can be represented in 10 bits 2's complement representation is

(a) -256 (b) -512

(c) -1024 (d) None of the above

[Turn over

(vii) Which of the following statement is correct?

(a) A XOR 0 = $\overline{A}$ (b) A XOR 0 =A

(c) A XNOR 0 = 1 (d) A XNOR 0 = A

(viii) 2's complement of binary number 0101 is _____.

(a) 1011 (b) 1111

(c) 1101 (d) 1110

(ix) The logic behind NOR gate is that it gives

(a) High output when both the inputs are low

(b) Low output when both the inputs are low

(c) High output when both the inputs are high

(d) None of the above

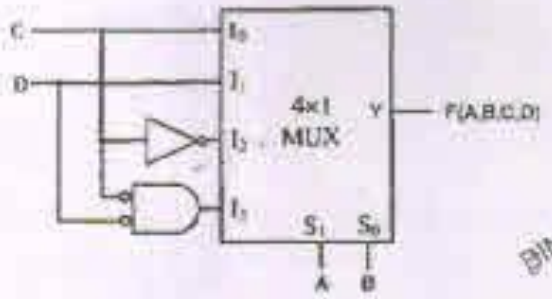
(x) In which of the following radix system, 123 is not a valid number

(a) Radix 10 (b) Radix 16

(c) Radix 8 (d) Radix 3

2. Answer any *three* of the following: (3 × 5 = 15)

(a) Find the Boolean function realized by the logic circuit shown below in SOP form. Also express the same expression in Standard SOP form.



(b) What is race around condition and how it can be avoided?

(c) Design a 4-bit Carry Look Ahead adder using full adder as basic building block.

(d) With neat diagram, explain the architecture of FPGA. Mention some of its applications.

3. (a) Design a 3-bit BCD to Excess-3 converter with neat diagram. (5)

(b) Write short note on any two of the following- (2 × 5 = 10)

(i) Flash ADC

(ii) R-2R Ladder Digital to Analog converter

(iii) Content Addressable Memory

4. (a) The Boolean function F(R, S, T) is expressed as- (3+3=6)

$F = \overline{R}S\overline{T} + R\overline{S}T + RST$

(i) Express F in the minimum SOP form using K-map.

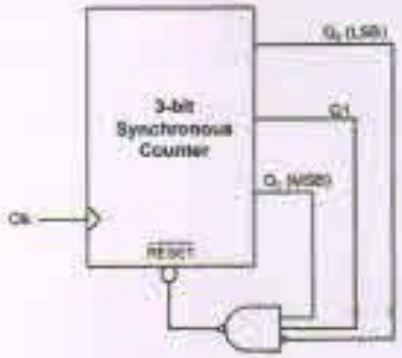
(ii) Express F in the minimum POS form.

(b) Design JK flip-flop using SR flip-flop. Mention some of the applications of D flip-flop. (4+2)

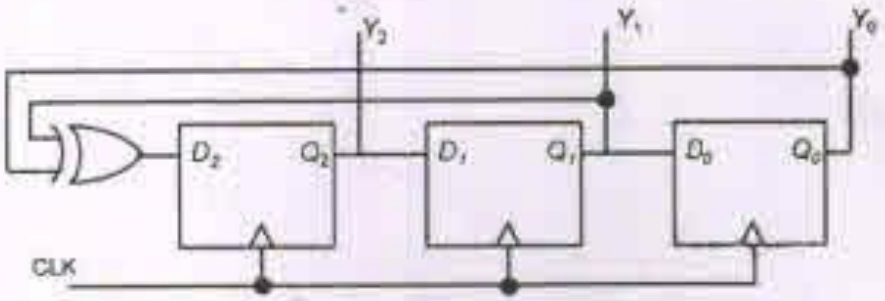
(c) Why gray codes are known as "self-reflecting codes"? (3)

5. (a) Design a 3-bit asynchronous up-down counter with neat diagram. (7)

(b) For the circuit shown in the figure, the delay of the bubbled NAND gate is 2ns and that of the counter is assumed to be zero. If the clock (Clk) frequency is 1 GHz, then calculate the modulus of the counter. (5)



(c) A three bit pseudo random number generator is shown. Initially the value of output Y = Y_2 Y_1 Y_0 is set to 111. What is the value of output Y after three clock cycles? (3)



6. (a) With neat diagram, explain the working of TTL NAND gate using Totem Pole output configuration. (7)

(b) Design the basic and universal logic gates using only 2:1 multiplexers. (5)

(c) Mention the differences between Mealy and Moore state machine. (3)