Total No. of printed pages = 2

EI 181305

Roll No. of candidate

5/3/22   2021

B.Tech. 3rd Semester End-Term Examination

EE, IE, EEE

DIGITAL ELECTRONICS

(New Regulations and New Syllabus)

Full Marks – 70   Time – Three hours

The figures in the margin indicate full marks

for the questions.

Answer question No. 1 and any *four* from the rest.

1. (a) Find Decimal equivalent of binary no $(1100.1011)_2$.   (1)
    (b) Find Binary equivalent of decimal no $(25.5)_{10}$.   (1)
    (c) Find Octal equivalent of decimal no $(249)_{10}$.   (1)
    (d) Find Hexadecimal equivalent of binary no $(10110011)_2$.   (1)
    (e) Find Octal equivalent of binary no $(11011100.101010)_2$.   (1)
    (f) Fill up the blanks by the next two Hexadecimal numbers 5E, 5F,
         _____, _____.   (1)
    (g) Find the GRAY CODE for binary $(1101101)_2$.   (1)
    (h) Find the binary equivalent of GRAY CODE $(1110101)_{GRAY\ code}$.   (1)
    (i) Subtract $(11100)_2$ from $(10011)_2$ by 2's complement method.   (2)

2. (a) Simplify the following expressions and get the minimized forms by using
         Boolean algebraic theorems.

         (i) $((AB' + ABC') + X(Y + XY'))'$

         (ii) $A(A' + C)(A'B + C')$ $(3 + 3 = 6)$

    (b) Derive the standard SOP and standard POS expressions for the following
         function :

         $f(A, B, C) = (A + BC)(B + C'A)$ (4)

    (c) Represent the following logical expression in a K-map and obtain the
         minimized expression from it.

         $f(A, B, C, D) = AB + AC' + C + AD + AB'C' + ABC$ (5)

[Turn over

3. (a) Obtain the minimized SOP expression for the following function by Quine McClusky's method :

$f(A, B, C, D) = \Sigma m (1, 2, 3, 7, 8, 9, 10, 11, 14, 15)$ (8)

(b) Starting from the Truth Table and with the help of k-map develop the logic expressions of a 2-bit digital comparator circuit. (3 + 4 = 7)

4. (a) What is a multiplexer? Implement the following Boolean function by using 8 : 1 multiplexer.

$f(A, B, C, D) = \Sigma m (0, 1, 3, 7, 9, 10, 11, 13, 14, 15)$ (2 + 6 = 8)

(b) What is the advantage of Master-Slave J-K flip flop over J-K fip flop? Explain the operation of Master-Slave J-K flip flop with a neat diagram. (2 + 5 = 7)

5. (a) Explain the operation of a full adder with a neat diagram. (4)

(b) What are half subtractor and full subtractor? (3)

(c) Explain how full adders can be used for both addition and subtraction of multibit numbers. (8)

6. (a) What is a register? Explain in details how a register works in PISO mode? (1 + 7 = 8)

(b) Draw the circuit of a modulus-16 Asynchronous Up-counter and explain its working principle. (7)

7. Write briefly about any *three* of the following: (3 × 5 = 15)

(a) RAM organization

(b) Parity generator and checker.

(c) Mod-7 counter

(d) 7-segment decoder

(e) ADC