Total No. of printed pages = 4

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ECE 142103

Roll No. of candidate | | | | | | | | | | |

2019

M.Tech.(ECE) 1st Semester End-Term Examination

DIGITAL IC DESIGN

(New Regulation)(W.e.f. 2018-19) &

(ASTU Syllabus)

Full Marks – 70 Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer Question No. 1 and any *four* from the rest.

1. Fill in the blanks: (10 × 1 = 10)

   (i) MOSFET is a ———— controlled device.

   (ii) A MOSFET can conduct at $V_{GS} = OV$ in ———— mode.

   (iii) The effective channel length of a MOSFET in saturation decreases with increase in ————.

   (iv) $R_{DS}(ON)$ of a MOSFET ———— with increase in V_{GS}.

[Turn over

(v) In constant field scaling, a parameter which is not scaled down is ————————.

(vi) AND terms are realized by ———————— connection of nMOS in PDN.

(vii) How may transistors are required to realize the function $F = AB + C$ using CMOS logic? ————————

(viii) Standard cell based design takes ———————— time than FPGA based design.

(ix) DRAM is widely used because ————————.

(x) Glitch in logic circuit ————————power dissipation.

2. (a) Draw the I-V characteristics of an n-channel MOSFET showing the different regions of operation. (7)

(b) Derive an expression for threshold voltage of MOSFET. (5)

(c) For a particular IC fabrication process, the trans-conductance parameter $\mu_n = 50\mu A/V^2$ and $V_{TH} = IV$. In an application in which $V_{GS} = V_{DS} = 5V$, a drain current of 0.8 mA is required for a device with a minimum length of $2\mu m$. What value of channel width must the design use? (3)

3. (a) What is channel length modulation? Explain with neat diagram. (5)

(b) Prove that pull up to pull down ratio of an nMOS inverter driven by another is 4:1. (5)

(c) Estimate the dynamic power dissipation in CMOS inverter. (5)

4. (a) What is calling in VLSI design? Explain its significance. Give the scaling factors for constant field model for the following: (6)

(i) Power supply voltages.

(ii) Gate oxide capacitance

(iii) Carrier densities in the channel

(iv) Power dissipation.

(b) In a CMOS inverter, assume that $\mu_n = 20\mu A/V^2$, $\left(\frac{W}{L}\right)_n = \frac{10}{1}$, $\mu_n = 0.4\mu_p$, $\left(\frac{W}{L}\right)_p = \frac{10}{1}$ and $V_{DD} = 5V$. The inverter dreives a load capacitance of 150pF. Find.

(i) high to low propagation delay.

(ii) low to high propagation delay.

(iii) what should be the dimension of the pMOS transistor such that both are to be equal. (6)

(c) Compare constant field scaling and constant voltage scaling. (3)

5. (a) Implement the logic function $f = ab + bc + ca$ using CMOS logic with as few transistors as possible. (5)

(b) Implement a 2:1 multiplexer using transmission gate. (5)

(c) What is pre-charge evaluate logic? Implement a 2 input NOR gate using pre-charge evaluate logic. (5)

6. (a) Why RAM is used as a cache memory? State the advantages of SRAM over DRAM. (5)

(b) Draw and explain the block diagram of a PLA based FSM implemented in MOS integrated circuit. (10)

7. Write short notes on any THREE of the following. (3 × 5 = 15)

(a) Domino CMOS logic

(b) Pass Transistor

(c) Back Gate Effect

(d) DRAM Cell.