Total No. of printed pages = 3

EC 131701 NR

Roll No. of candidate | | | | | | | | | | |

8/2/2021

B.Tech. 7th Semester End-Term Examination

ECE + AEI

LINEAR INTEGRATED CIRCUITS

(New Regulation)

Full Marks – 70 Time – Three hours

The figures in the margin indicate full marks for the questions.

GROUP – A

1. Answer *all* the question : (10)

(i) If one of the input and output of an ideal op-amp is 2V and 12V and the gain is 3, then the other input of the ideal op-amp is (8V / 4V / –4V / –2V)

(ii) (Infinite voltage gain / Infinite bandwidth / Infinite output resistance / Infinite slew rate) is not the ideal characteristic of an op-amp.

(iii) In ideal Differential amplifier, if same signal is given to both inputs, then output will be (same as input / double the input/ Not equal to zero / zero)

(iv) Level shifter in op-amp internal circuit is to (Adjust DC voltage / Increased impedance / Provide high gain / Decrease input resistance)

(v) CMRR of a differential amplifier can be improved by decreasing (Differential voltage gain / Common mode voltage gain / Both / None of these)

(vi) An inverting amplifier with gain of 1 have different input voltage 1.5V, 2.4V and 3.6V. The output voltage will be (3.9V / 7.5V / –7.5V / –3.9V)

(vii) For an ideal comparator the value of the response time is (Zero / Unity / Infinite / unpredictable)

[Turn over

(viii) The feedback factor of voltage follower circuit is (zero / unity / Infinity / Between zero and one)

(ix) (V to I converter / Comparator / Precision rectifier / Instrumentation amplifier) is a non linear application of op-amp.

(x) In an inverting ideal differentiator (R /L / C /Diode) is present in the feedback path.

GROUP – B

Answer *any four* questions.

2. (a) Derive A_f, R_{if} R_{of}, BW for an inverting mode negative feedback amplifier with a 741 OpAmp having R1 = 1 K ohm and Rf = 40 K ohm. (6)

(b) Draw the internal block diagram of Op-Amp. Explain each block. (6)

(c) Explain the significance of virtual ground in an op-amp. (3)

3. (a) What is input and output offset? How are they compensated? (5)

(b) With a neat circuit diagram explain the working of voltage to current converter. (6)

(c) Define Slew rate. An operational amplifier has a slew rate of 4v/µs. Determine the maximum frequency of operation to produce distortion less output swing of 12V. (4)

4. (a) Draw the schematic of a linear IC triangular waveform generator and explain the circuit operation. (8)

(b) Draw the circuit diagram of a comparator. Mention its application. (7)

5. (a) Explain the operation of the following circuits (10)

(i) Zero cross detector

(ii) Clipper and clamper circuit.

(b) Describe the process of hysteresis generation in Schmitt trigger circuit. (5)

6. (a) With a neat circuit diagram explain the working of linear voltage regulator using operational amplifier. (6)

(b) Design a second order low pass filter using operational amplifier for the upper cut off frequency of 2 KHz. Assume the value of the capacitor to be 0.1 µF. (6)

(c) Define Capture range and Lock range of PLL. (3)

7. (a) Describe the 555 Timer IC. Design a Astable Multivibrator Circuit to generate output Pulses of 50% duty cycle using 555 Timer IC, with $C = 0.01\ \mu F$, Frequency as 4 KHz. (10)

(b) Calculate the value of the LSB, MSB, and full scale output for an 8-bit DAC for the 0 to 12V range. (5)