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EC 131702 NR

Roll No. of candidate | | | | | | | | | | |

2312h2 **2021**

B.Tech. 7th Semester End-Term Examination

ECE

VHDL AND DIGITAL SYSTEM DESIGN

(New Regulation)

Full Marks – 70 Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer question No. 1 and any *four* from the rest.

1. Choose the correct answer : (10 × 1 = 10)

(i) What is the full term of VHDL?

(a) Very High Definition Language

(b) Very High Speed Integrated circuit Hardware Description Language

(c) Very High Description Language

(d) Very High Speed Scaling Hardware Describing Language

(ii) Which of the following is the basic building block of a design?

(a) Architecture (b) Entity

(c) Process (d) Package

(iii) In composite data type of VHDL, the record type comprises the elements of _____data types.

(a) Same (b) Different

(c) Both (a) and (b) (d) None of the above

[Turn over

(iv) Which of the following circuit can't be described without using a process statement?

(a) Multiplexer (b) D flip-flop

(c) Decoder (d) Comparator

(v) A process must have all the _____ signals in its sensitivity list.

(a) Used (b) Input

(c) Output (d) Declared

(vi) Which wait statement does follow a condition?

(a) wait for (b) wait

(c) wait until (d) wait on

(vii) Which is the default delay in VHDL?

(a) Transport delay (b) Delta delay

(c) Inertial delay (d) Wait statements

(viii) How to declare a constant in VHDL?

(a) CONSTANT name : type := value;

(b) CONSTANT name := value;

(c) CONSTANT name := type := value;

(d) CONSTANT name := type : value;

(ix) Which of the following is true about packages?

(a) Package is collection of libraries

(b) Library is collection of packages

(c) Package is collection of entities

(d) Entity is collection of packages

(x) In VHDL, LOOP is a _____ statement.

(a) Concurrent (b) Sequential

(c) Procedural (d) Functional

2. (a) What are the different modes associated with a ports. (4)

(b) Define sensitivity list? Explain its significance in a process (3)

(c) What is the need of configuration in VHDL? Explain in details (3)

(d) Write the VHDL code for BCD to 7 segments using CASE statement. (5)

3. (a) List different data objects used in VHDL with examples showing how those are declared in VHDL program. (5)

(b) Write the VHDL code for a T flip flop having asynchronous reset and clear signal.

Using the above T flip-flop as component, design a 4 bit up counter. Use GENERATE statement to write the VHDL code. (10)

4. (a) Write the VHDL code to design an ALU that can perform all arithmetic and logical operations (5)

(b) What are the advantages of subprogram? Write the differences between PROCEDURE and FUNCTION with examples. (5)

(c) Compare transport delay and inertial delay with example. (5)

5. (a) Write the structural description to realize the Boolean expression given below $Y = \overline{(\overline{A} + \overline{B}) \cdot (C + D)}$. (5)

(b) Define and explain component declaration and component instantiation with example. (5)

(c) What are the shift operators available in VHDL? Give examples of each type. (5)

6. (a) What is resolution function? What is the need of resolution function? (5)

(b) Write the VHDL code for sequence detector to detect the sequence " 101". (10)

7. Write short notes on any *three* : (3 × 5 = 15)

(a) FPGA

(b) Package and Library

(c) Mealy and Moore state machine

(d) Test bench

(e) Design methodology