Total No. of printed pages = 2

EC 131703 NR

Roll No. of candidate | | | | | | | | | | |

28/2/22 2021

B.Tech. 7th (New) Semester End-Term Examination

ECE

VLSI DESIGN

Full Marks – 70 Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer question No. 1 and any *four* from the rest.

1. Answer the following questions : (5 × 2 = 10)
   (a) Define g_m of MOS transistor.
   (b) Define scaling and explain it.
   (c) Draw 2-bit comparator.
   (d) What is switch logic?
   (e) Mention about SRAM and its usage.

2. (a) Explain with neat diagrams the various NMOS fabrication technology. (10)
   (b) Compare depletion and enhancement type MOSFET. (5)

3. (a) Derive the expression for transfer characteristics of CMOS Inverter. (10)
   (b) Discuss and derive expression for channel length modulation. (5)

4. (a) Draw the circuit diagram; stick diagram and layout for CMOS inverter. (10)
   (b) Discuss dynamic power dissipation due to charging and discharging capacitances of a CMOS inverter. (5)

[Turn over

5. (a) Describe the following:

(i) Transmission gate logic

(ii) Domino Logic. (10)

(b) Design $\overline{F} = (A + B) + (C + D)EF$ using pseudo-NMOS and CMOS logic. (5)

6. (a) Explain different capacitances present in CMOS design. (8)

(b) Explain λ-based Design Rules in VLSI circuit Design. (7)

7. (a) Write a program to implement full adder using VHDL. (10)

(b) Write a note on the different parameters influencing low power design. (5)