Total No. of printed pages = 4

ECE 181702

Roll No. of candidate | | | | | | | | | | |

19/12/22 2021

B.Tech. 7th Semester End-Term Examination

ECE + ETE

VLSI SYSTEM DESIGN

**(New Regulation w.e.f 2017-18 &
New Syllabus w.e.f. 2018-19)**

Full Marks – 70 Time – Three hours

The figures in the margin indicate full marks
for the questions.

Answer question No. 1 and any *six* from the rest.

1. (10 × 1 = 10)

(i) MOSFET can be used as a
- (a) Current controlled capacitor
- (b) Voltage controlled capacitor
- (c) Current controlled inductor
- (d) Voltage controlled inductors

(ii) Thermal runaway is not possible in FET because as the temperature of FET increases
- (a) The mobility decreases
- (b) The transconductance increases
- (c) The drain current increases
- (d) None of the above

(iii) The drain current of a MOSFET in saturation is given by $I_{ds} = K(V_{gs} - V_{th})(V_{gs} - V_{th})$ where K is a constant. The magnitude of the transconductance g_m is
- (a) $K(V_{gs} - V_{th})(V_{gs} - V_{th})/V_{ds}$
- (b) $2K(V_{gs} - V_{th})$
- (c) $I_{ds}/(V_{gs} - V_{th})$
- (d) $K(V_{gs} - V_{th})(V_{gs} - V_{th})/V_{gs}$

[Turn over

(iv) A silicon wafer has 100nm of oxide on it and is inserted in a furnace at a temperature above 1000 degree c for further oxidation in dry oxygen. The oxidation rate

(a) Is independent of current oxide thickness and temperature?

(b) Is independent of current oxide thickness but depends on temperature

(c) Slow down as the oxide grows

(d) Is zero as the existing oxide prevents further oxidation

(v) A gate to drain-connected enhancement mode MOSFET is an example of

(a) An active load (b) A switching device

(c) A four-terminal device (d) A three-terminal device

(vi) The effective channel length of a MOSFET in a saturation decreases with increase in

(a) Gate voltage (b) Drain voltage

(c) Source voltage (d) Body voltage

(vii) The MOSFET switch in its on-state may be considered equivalent to

(a) Resistor (b) Inductor

(c) Capacitor (d) Battery

(viii) In a transconductance, the device output

(a) Voltage depends upon the input voltage

(b) Voltage depends upon the input current

(c) Current depends upon the input voltage

(d) Current depends upon the input current

(ix) In a MOSFET operating in the saturation region, the channel length modulation effect causes

(a) An increase in the gate-source capacitance

(b) A decrease in the Transconductance

(c) A decrease in the unity-gain cut-off frequency

(d) A decrease in the output resistance

(x) An n-type silicon bar 0.1 cm long and 100 π m^2 in cross-sectional area has a majority carrier concentration of $5 \times 10^{20}/m^3$ and carrier mobility is $0.13 m^2$ /V-s at 300k. if the charge of an electron is 1.6×10^{-19} Coulomb, then the resistance of the bar is

(a) 10^6ohm (b) 10^{-1} ohm

(c) 10^{-4} ohm (d) 10^4 ohm

2. Using appropriate sketches show how a wet-etching photolithography process works using:

(a) Positive resists.

(b) Negative resist.

(c) Remove silicon dioxide insulator.

(d) Remove aluminium metallization. (4 × 2.5 =10)

3. (a) What is epitaxial? Why it is necessary in IC fabrication?

(b) Explain the deal grove method. (5+5=10)

4. Describe the fabrication process of a capacitor with neat diagrams and steps. (10)

5. What do you mean by transconductance in a MOS device? Derive the question of MOS transconductance. Draw the flowing

(a) curve of g_m vs $V_{gs} - V_{th}$ h when W/L constant.

(b) curve of g_m vs I_{DS} when W/L constant.

(c) curve of g_m vs $V_{gs} - V_{th}$ when I_{DS} constant . (2+5+3=10)

6. Describe the various ways how MOS based inverter can be built. (4 × 2.5 =10)

7. Explain CMOS inverter transfer characteristics with a neat diagram. What is noise margin of an inverter? Derive with neat diagram and equations? (6+4=10)

8. Draw the stick diagram for the given logic

$X = \overline{AB + C}$ (10)

9. Draw the layout diagram for the given logic $X = \overline{A + B}$. (10)

10. Prove the scaling factors for the following: (4 × 2.5 =10)

(a) Gate capacitance

(b) Channel resistance.

(c) Maximum operating frequency.

(d) Switching energy per gate.

11. Write short notes: (any *two*) (2×5=10)

(a) Bi-CMOS logic.

(b) LOCOS

(c) Second order effect of MOSFETs.

(d) Enhancement mode and depletion mode N-MOS.

(e) Czochralski process.