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MCA 202101

Roll No. of candidate

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M.C.A. 1st Semester End-Term Examination

COMPUTER ORGANIZATION AND ARCHITECTURE

New Regulation (w.e.f. 2020-21) &

New Syllabus (w.e.f. 2020-21)

Full Marks – 70 | Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer question No. 1 and any *four* from the rest.

1. Answer the following MCQ: (10 × 1 = 10)

(i) A Stack organization computer uses instruction of

(a) Indirect addressing (b) Two addressing

(c) Zero addressing (d) Index addressing

(ii) If the main memory is of 8K bytes and the Cache memory is of 2K words. It uses associative mapping then each word of cache memory shall be

(a) 10 bits (b) 20 bits

(c) 16 bits (d) 32 bits

(iii) A group of bits that tell the computer to perform a specific operation is known as

(a) Instruction code (b) Accumulator

(c) Micro operation (d) Register

(iv) The communication between the components in a micro computer takes place via the Address and ————

(a) Data bus (b) I/O bus

(c) Address bus (d) Control bus

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(v) An address in main memory is called

(a) Physical address (b) Logical address

(c) Memory address (d) Word address

(vi) The performance of Cache memory is frequently measured in terms of quantity called

(a) Miss ratio (b) Hit ratio

(c) Latency ratio (d) Read ratio

(vii) An interface that provides I/O transfer od data directly to and from the memory unit and peripheral is termed as

(a) DDA (b) Serial interface

(c) BR (d) DMA

(viii) The maximum addressing capacity of a micro processor which uses 16 bit database and 32 bit address base is

(a) 64K (b) 2GB

(c) 4GB (d) none of these

(ix) Memory unit accessed by content is called

(a) Read only memory (b) Programmable memory

(c) Virtual memory (d) Associative memory

(x) In computer's subtraction is carried out given by

(a) 1's complement method

(b) 2's complement method

(c) Signed magnitude method

(d) BCD subtraction method

2. (a) Evaluate X = (P*Q) * (R+S) using two address instruction and one address instruction. (6)

(b) What are 2's complement and 1's complement? Explain. (3)

(c) What is logical shift operation? What is the value of following register A after logical shift right operation? (1+2)

(d) What do you mean by computer organization and architecture? (3)

3. (a) What is a common bus system? Explain the main types of buses in a computer system. (2+3)

(b) Draw a diagram of a CPU with single bus organization. In that diagram explain the need of each component. (6)

(c) What is an Instruction set architecture? Briefly explain all the phases involved in the instruction execution cycle? (1+3)

4. (a) Briefly explain the difference between hardwired control and microprogrammed control? Explain control memory and control words. (4+2)

(b) Is the interrupt-initiated input-output mode of data transfer is better than the programmed input-output mode? Give reasons to support your answer. (4)

(c) What is the DMA mode of data transfer? Explain cycle stealing and burst mode. (3+2)

5. (a) Briefly explain the daisy-chaining mechanism in detail. (5)

(b) Briefly explain the difference between synchronous and asynchronous data transfer? Write the advantages of the strobe control method over the handshaking method of data transfer. (5)

(c) What is content addressable memory? What is its importance in the computer system? (2+3)

6. (a) Write short notes of the following (Any *two*): (5+5)

(i) Booth's multiplication algorithm

(ii) Virtual memory

(iii) RISC and CISC

(b) Write the control control steps for executing the following instruction ADD R1, (R2)

Consider the CPU using single bus organization. (5)

7. (a) What is the need for cache memory in a computer system? Explain the advantages of the direct mapping technique in detail. (1+5)

(b) What do you mean by addressing mode? Explain the benefits (1+2)

(c) From the following figure find out the effective address for the following. Consider PC=200, R1=400, XR=100 (PC= Program counter, R1= processor register, XR= index register) (6)

(i) Direct mode

(ii) Indirect mode

(iii) Register mode

(iv) Immediate mode

(v) Relative mode

(vi) Register indirect mode

200	Load to Ac	Mode
201	Address = 500	
202	Next instruction	
399	450	
400	700	
500	800	
600	900	
800	300	