Total No. of printed pages = 3

MCA 202101

Roll No. of candidate | | | | | | | | | | |

2013/2021

M.C.A. 1st Semester End-Term Examination

COMPUTER ORGANIZATION AND ARCHITECTURE

(New Regulation & New Syllabus)

Full Marks – 70 Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer question No. 1 and any *four* from the rest.

1. Answer the following questions : (10 × 1 = 10)

(i) Consider a cache memory system with 4096 primary memory blocks, 128 cache memory blocks and 16 words available in each block. In direct mapping technique, how many bits are needed to specify TAG in this organization?

(a) 4 (b) 5

(c) 7 (d) None of these

(ii) ADMA controller transfers 16-bitwords to memory using cycle stealing. The words are assembled from a device that transmits characters at a rate of 2400 characters per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per second. By how much will the CPU be slowed down because of the DMA transfer? [Two characters of 8 bits each are packed into 16 bit words]

(a) 0.35% (b) 0.12%

(c) 0.91 (d) None of these

(iii) Consider a cache memory system with 4096 primary memory blocks, 128 cache memory blocks and 16 words available in each block. In direct mapping technique, how many bits are needed to specify BLOCK field in this organization?

(a) 128 (b) 7

(c) 5 (d) None of these

[Turn over

(iv) If the word length of a machine is 64 bit, according to byte address ability, successive words are located at addresses

(a) 0,1,2,3 (b) 0,8,16,24

(c) 0,4,8,12 (d) None of these

(v) Which of the following value is never possible for cache miss?

(a) 0.5 (b) 1.14

(c) 0.4 (d) None of these

(vi) Which of the following is used to temporarily hold instruction inside the CPU?

(a) PC (b) IR

(c) Multiplexer (d) None of these

(vii) What is RISC?

(a) Remote Interface System Computer

(b) Remote Intranet Secured Connection

(c) Runtime Instruction Set Compiler

(d) Reduced Instruction Set Computer

(viii) If certain processor support only immediate and direct addressing mode, which of the following programming language feature cannot be implemented on this processor?

(a) Records (b) Arrays

(c) Pointers (d) All of the Above

(ix) Every instruction cycle consists of

(a) Fetch Cycle (b) Execute Cycle

(c) Both (a) and (b) (d) None of these

(x) When a program is being executed its Program Counter contains

(a) Number of instructions in the current program that have already been executed

(b) The total number of instructions in the program being executed

(c) Memory address of the instruction that is being currently executed

(d) Memory address of the instruction that is to be executed next

2. (a) What is 'locality of reference'? Explain how 'locality of reference' helps in implementation of cache memory. (6)

(b) How virtual address is different from physical address? Explain the concept of virtual memory in detail with diagram. (9)

3. (a) Explain hardwired control mechanism for generation of control signals. (7)

(b) A virtual memory system has an address space of 8k words, a memory space of 4k words and page and block size of 1k words. The following page reference changes occur during a given time interval: (8)

4 2 0 1 2 6 1 4 0 1 0 2 3 5 7

[if the same page is referenced again, it is not listed twice]

Determine the four pages that are resident in memory after each page reference change, if the replacement algorithm used is LRU.

4. (a) It is necessary to transfer 256 words from a magnetic disk to a memory section starting from the address 1230. The transfer is by means of DMA. What are the initial values that the CPU must transfer to the DMA controller? Give the step-by-step account of the actions taken during the input of the first two words. (9)

(b) Explain micro programmed control mechanism for generation of control signals. (6)

5. (a) How MAR is different from MDR? Explain why the connection between MAR and Memory is unidirectional but that of MDR and Memory bi–directional. (6)

(b) Describe Single Bus Structure inside CPU in detail with diagram. (9)

6. (a) Explain Direct mapping and Block Set Associative mapping techniques of Cache memory in detail with diagram. (9)

(b) Describe the concept of Associative Memory in detail. (6)

7. Write short note on $(3 \times 5 = 15)$

(a) Associate Mapping of Cache Memory

(b) Associative Memory

(c) Double bus structure inside CPU
