Total No. of printed pages = 3

CSE 181303

15/2/23

Roll No. of candidate ☐☐☐☐☐☐☐☐

2023

B.Tech. 3rd Semester End-Term Examination

DIGITAL SYSTEMS

Full Marks – 70   Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer Question No. 1 and any *four* from the rest.

1. Answer the following (MCQ/ Fill in the blanks) : $(10 \times 1 = 10)$

    (i) Convert the binary number $(01011.1011)_2$ into decimal
        (a) $(11.6875)_{10}$ (b) $(11.5874)_{10}$
        (c) $(10.9876)_{10}$ (d) $(10.7893)_{10}$

    (ii) The following hexadecimal number $(1E.43)_{16}$ is equivalent to
        (a) $(36.506)_8$ (b) $(36.206)_8$
        (c) $(35.506)_8$ (d) $(35.206)_8$

    (iii) Convert $(0.345)_{10}$ into an octal number
        (a) $(0.16050)_8$ (b) $(0.26050)_8$
        (c) $(0.19450)_8$ (d) $(0.24040)_8$

    (iv) The excess-3 code for 597 is given by —————.
        (a) 100011001010   (b) 100010100111
        (c) 010110010111   (d) 010110101101

    (v) 2's complement of 11001011 is —————.
        (a) 01010111   (b) 11010100
        (c) 00110101   (d) 11100010

[Turn over

(vi) The gates required to build a half adder are —————.

    (a) EX-OR gate and NOR gate   (b) EX-OR gate and OR gate

    (c) EX-OR gate and AND gate   (d) EX-NOR gate and AND gate

(vii) The expression $Y = AB + BC + AC$ shows the ————— operation.

    (a) EX-OR   (b) SOP

    (c) POS   (d) NOR

(viii) The expression $Y = (A + B)(B + C)(C + A)$ shows the ————— operation.

    (a) AND   (b) POS

    (c) SOP   (d) NAND

(ix) Each product term of a group, $w'.x.y'$ and $w.y$, represents the ————— in that group.

    (a) Input   (b) POS

    (c) Sum-of-Minterms   (d) Sum of Maxterms

(x) Which of the following logic families has the highest maximum clock frequency?

    (a) S-TTL   (b) AS-TTL

    (c) HS-TTL   (d) HCMOS

2. (a) State and prove Demorgan's theorem. (5)

   (b) Compare Combinational circuits with sequential circuit. (5)

   (c) Design 3-bit Binary to Gray code converter. (5)

3. (a) Using a K map simplification process determine the logic expression that will active the segment from 0 to 9. (10)

   (b) Draw the 4×16 decoder circuit using two 3×8 Decoders. (5)

4. (a) Draw and explain a neat circuit diagram of the BCD adder using IC 7483. (5)

   (b) Minimize the following expression using quine McCluskey Technique
   $F(A, B, C, D) = \Sigma m(1, 3, 7, 11, 15) + d(0, 2, 5)$. (5)

   (c) Implement the following function using a single 8 : 1 multiplexer
   $f(A, B, C, D) = \Sigma m(2, 3, 5, 7, 8, 9, 12, 13, 14, 15)$. (5)

5. (a) Explain a full adder circuit using PLA having three inputs, 8-product terms, and two outputs. (5)

   (b) What are shit registers? How are they classified? Explain the working of any type of shift register. (10)

6. (a) Explain Master slave JK Flip-flop. (5)

   (b) Convert T flip-flop to D Flip-flop. (5)

   (c) Explain about ripple counter. (5)

7. (a) Construct the PROM using the conversion from BCD code to Excess-3 code. (5)

   (b) What is an ADC? Using which theorem it works, explain. (5)

   (c) Draw the MOD-2 counter. (5)

8. (a) Write the difference between PROM, PLA and PAL. (5)

   (b) Write about the following : (any *two*) (5 + 5 = 10)

      (i) Transistor – Transistor Logic (TTL)

      (ii) Emitter – Coupled Logic (ECL)

      (iii) CMOS Logic.

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