Total No. of printed pages = 3

ECE 181303

13/2/23

Roll No. of candidate | | | | | | | | | | |

2023

B.Tech. 3rd Semester End-Term Examination

Electronics and Telecommunication Engineering

DIGITAL CIRCUITS

(New Regulation and New Syllabus)

Full Marks – 70 Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer Question No. 1 and any *four* from the rest.

1. Answer the following (MCQ/ Fill in the blanks) : $(10 \times 1 = 10)$

(i) Which of the following is correct for Digital Circuits?

(a) Less susceptible to noise or degradation in quality

(b) Use transistors to create logical gates to perform Boolean logic

(c) Easier to perform error detection and correction with digital signal

(d) All of the mentioned

(ii) Which of the following is a Universal set of logic gate(s)?

(a) {NAND} (b) {NOR}

(c) {AND, OR, NOT} (d) All of the above

(iii) Which of the following options comes under the non - saturated logic family in Digital Electronics?

(a) Emitter – coupled Logic (b) High – Threshold Logic

(c) Integrated – injection Logic (d) Diode – Transistor Logic

(iv) What is a switching function that has more than one output called in Digital Electronics?

(a) Multi – gate function (b) Multi – logic function

(c) Multiple – gate function (d) Multiple – output function

[Turn over

(v) In which form of Boolean/logic function is each term known as minterm?

(a) SOP (b) POS

(c) Hybrid (d) Both (a) and (b)

(vi) Which gates in Digital Circuits are required to convert a NOR-based SR latch to an SR flip-flop?

(a) Two 2 input And gates (b) Two 3 input AND gates

(c) Two 2 input OR gates (d) Two 3 input OR gates

(vii) When does a negative level triggered flip-flop in Digital Electronic changes its state?

(a) When the clock is negative (b) When the clock is positive

(c) When the inputs are all zero (d) When the inputs are all one

(viii) Pin No. 14 of the 7400 IC is

(a) Input (b) Output

(c) V_{CC} (d) Ground

(ix) A + A.B is equal to

(a) A or B b) A.B

(c) B (d) A

(x) What will be the frequency of the output from a JK flip – flop, when J = 1, k = 1 and a clock with pulse waveform is given?

(a) Half the frequency of clock input

(b) Equal to the frequency of clock input

(c) Twice the frequency of clock input

(d) Independent of the frequency of clock input

2. (a) Construct BCD adder using two 4-bit binary parallel adder and logic gates. Explain its operation. (10)

(b) Explain 4-bit magnitude comparator (5)

3. (a) Construct a 5 × 32 decoder with four 3 × 8 decoder and a 2 × 4 decoder. Use block diagram construction only. (8)

(b) Implement Boolean function F (A, B, C, D) = Σm (0, 1, 3, 4, 8, 9, 15) using 8:1 multiplexer. (7)

4. (a) Design 3-bit binary counter using T-flip-flop and discuss its operation with state table and timing diagram. (7)

(b) Discuss "Digital IC logic families" and characteristics of basic gate in each family. (8)

5. (a) Realise J-K flip-flop using S-R flip-flop and gates. Show the excitation table, K-map and the realized circuit diagram. (7)

(b) Describe digital multiplexer in detail using suitable example. Obtain an 8 × 1 multiplexer with a dual 4 – line to 1 – line multiplexers having separate enable inputs but common selection lines. Use block diagram construction. (8)

6. Write short notes (any *three*) (5 + 5 + 5 = 15)

(a) Full adder.

(b) Read – Only Memory (ROM)

(c) TTL

(d) Complementary MOS (CMOS)

7. Implement Boolean functions : (5 + 5 + 5 = 15)

(a) F = (A + B') (CD + E) using only NAND gates.

(b) F = A (B + CD) +BC' with only NOR gates.

(c) F = $x'y + xy'$ using only four NAND gates.