Total No. of printed pages = 3										
ECE 181501										
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B.Tech. 5th Semester End-Term Examination										
EEE, ECE, ETE, PEIE										
MICROPROCESSOR AND EMBEDDED SYSTEM										
(New Regulation/New Syllabus)										
						Time - Three hours				
The figures in the margin indicate full marks for the questions. Question no. 1 is compulsory and answer any four question no.2 to 7										
1.	1. Answer the following questions: $(10 \times 1 = 10)$									
	(i) The address bus width of a microprocessor which is capable 64k bytes of memory is				s capable 64k bytes of the					
		(a)	8	and the same	(b)	12				
		(c)	16		(d)	20				
	(ii)	The	address bu	s of any microp	rocessor i	is always bi	directional			
	17.	(a)	True		(b)	False				
	(iii)			CATEDORICA CONTRACTOR CONTRACTOR CONTRACTOR	the second second		um possible number of apped I/O technique			
		(a)	64	Sew by Tr	(b)	256				
		(c)	512		(d)	65536				
	(iv)	An	opcode is							
		(a)	Operand a	ddress			Private a s			
		(b)	Data on w	hich operation	is perform	ned				
		(c)	Operation	to be performe	d					

(d) None of these

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(v)	Consider the following registers								
	(1) Accumulator and flag regis	ter							
	(2) B and C register								
	(3) D and E register	WILL ST							
	(4) H and L register								
	Which of these 8-bit registers of 8085 microprocessor can be paired together to make a 16- bit register?								
	(a) 1,3 and 4	(b)	2,3 and 4						
*	(c) 1,2 and 3	(d)	1,2 and 4						
(vi)	ALE stands for								
	(a) Address Logic Enable	(b)	Arithmetic Latch Enable						
	(c) Address Latch Enable	(d)	Arithmetic Logic Enable						
(vii)	me arithmetic operations, then the								
	(a) PSW	(b)	SP						
	(c) DPTR	(d)	PC						
(viii)	How are the status of the carry, auxiliary carry and parity flag affected if the write instruction MOV A, #9C ADD A, #64H								
	(a) CY=0, AC=0, P=0	(b)	CY=1, AC=1, P=0						
	(c) CY=0, AC=1, P=0	(d)	CY=1, AC=1, P=1						
(ix)	JZ, JNZ, instructions checked content of register.								
	(a) DPTR	(b)	B						
	(c) A	(d)	PSW						
(x)	To initialize any port as an output port what value is to be given to it?								
	(a) 0 × FF	(b)	0×00						
	(c) 0 × 01	(d)	A port is by default an output port						
(a)	Explain Hardware Model and I with neat diagrams.	Progran	aming Model of 8085 Microprocessor (4 + 4 = 8)						
(b)	Draw the 8085 Flag register. Explain the operation of each flag in the register. $(2+5=7)$								
(a)	Classify 8085 instructions on th	Classify 8085 instructions on the basis of its different functions. (5)							
(b)	Data byte 32H is stored in register B and data byte 88H is stored accumulator. Show the contents of registers B, C and accumulate execution of the following two instructions:								
	MOV A, B		BINA CHOWDHURY CENTRAL LIBRARY (GIMT & GIPS)						
	MO V C, A		Azara, Hatkhowapara, Guwahati -781017 (3)						
(c)	Write an assembly language prolocation starting from 8050 to a	ogram t nother l	o transfer a block of 10 data stored in						

2.

3.

4.	(a)	If the memory chip size is 2048 × 8 bits, how many chips are required to make up 16Kbyte memory? (3)
	(b)	List the sequence of events that occur when 8085 executes CALL instruction with an example. (5)
	(c)	Draw the timing diagram of the instruction MVI A, 32H. (7)
5.	(a)	Define the following terms $(3 \times 1 = 3)$
		(i) Instruction Cycle
		(ii) Machine Cycle
		(iii) T State
	(b)	Explain the multiple interrupts and priorities of 8085 microprocessor. Draw the interrupt structure of 8085. (5)
	(c)	What are the control signals necessary in the memory mapped I/O? (2)
	(d)	4 switches are connected with 8085 through 8255 write an assembly language program that will read the status of these switches and will display it in a series of LED conceited with display with 8255. (5)
6.	(a)	What are the addressing modes supported by 8051? (5)
	(b)	Differentiate the given 8051 instructions: MOVC and MOVX. (2)
	(c)	Write an assembly language program to perform multiplication of two 8—bit numbers using 8051 instruction set. (8)
7.	Wri	te short notes on any <i>three</i> of the following topics. $(3 \times 5 = 15)$
T.	(a)	Direct Memory Access
	(b)	8255 PPI BINA CHOWEHURY CENTRAL LIBRARY (GIMT & GIPS) Azara, Hatkhowapara,
	(c)	Cache Memory Guwahati -781017
	(d)	RISC and CISC processor
	(e)	ARM Microcontroller.