Total No. of printed pages = 2

ECE 181702

Roll No. of candidate | | | | | | | | | | |

31/12/2022

2022

B.Tech. 7th Semester End-Term Examination

ECE + ETE

VLSI SYSTEM DESIGN

(New Regulation w.e.f 2017 – 18 & New Syllabus w.e.f 2018 – 19)

Full Marks – 70 Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer Question No. 1 and any *four* from the rest.

1. Fill in the blanks : (10 × 1 = 10)
   (a) The V_{ds} is _____ (lesser/greater) than $(V_{gs} - V_t)$ in MOSFET for non-saturated region of operation.
   (b) As source drain voltage increases, channel depth _____ (increases/decreases).
   (c) The photoresist layer exposed to _____ light during MOS fabrication.
   (d) BiCMOS has low power dissipation _____ (true/false).
   (e) CMOS is _____ (unidirectional/bidirectional).
   (f) The _____ colour is used for implant in stick diagram.
   (g) In λ – based design rules, the spacing between two diffusion layers is _____.
   (h) Propagation time is directly proportional to _____.
   (i) The subsystem of the circuits should have _____ (minimum/maximum) interdependence.
   (j) The power dissipation is directly proportional to square of _____.

2. (a) What are the steps involved in IC fabrication. (3)
   (b) Explain the nMOS fabrication process with suitable diagram. (7)
   (c) Draw the circuit schematic and stick diagram for the three input NAND Gate. (2+3 = 5)

[Turn over

3. (a) Explain briefly about sheet resistance. (3)

(b) Derive the expression for sheet resistance for nMOS transistor and find the same for a minimum size nMOS transistor. (2+2 = 4)

(c) State the λ– based design rules. Draw the layout diagram for the given logic $Y = \overline{A.B}$. (2+6 = 8)

4. (a) What is channel length modulation of MOS device? (3)

(b) What is transistor sizing? With expression explain in short the dynamic power dissipation in CMOS. (2+3 = 5)

(c) What is scaling? How it enhance device parameter. Derive the scaling factors for the device parameters (7)

(i) Gate Capacitance

(ii) Current density and

(iii) Power Dissipation per Gate.

5. (a) What is Body effect? (2)

(b) What is pass transistor and transmission gate? Explain how switch logic can be implemented using Pass transistors. (3+5 = 8)

(c) An nMOS transistor is operating in saturation region with the following parameters $V_{GS} = 5V$; $V_{tn} = 1.2V$; $W/L = 110$; $\mu_n C_{ox} = 110\mu A/V^2$. Find transconductance of the device. (5)

6. (a) Define Fan – in and Fan – out. (2)

(b) Find the worst-case parasitic delay of an n-input NOR gate. (5)

(c) With neat circuit diagram and truth, table explain the operation of Manchester carry chain adder. (8)

7. (a) Discuss the single stuck – at fault model. (5)

(b) What is logical effort? Find the logical effort of 2-input NAND gate. (5)

(c) Explain the operation of three transistor dynamic RAM cell (5)