Total No. of printed pages = 3

EI 181303

15/2123

Roll No. of candidate | | | | | | | | | | |

2023

B.Tech. 3rd Semester End-Term Examination

ANALOG ELECTRONICS

(New Regulation and New Syllabus)

Full Marks – 70 Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer question No. 1 and any *four* questions among questions 2 to 7.

(10 × 1 = 10)

1. (i) When a diode is forward biased then electrons moves from P region to N region. Is it True or False?

   (ii) A forward biased diode cannot be used as voltage regulator. Is it True or False?

   (iii) Zener breakdown of a PN junction diode occurs due to ———— (Write exact reason)

   (iv) When J_E is forward biased and J_C is forward biased then a BJT operates in (Write region of operation)

   (v) The current in the base of a BJT is mainly due to the recombination of electrons and holes. Is it True or False?

   (vi) In a trans conductance amplifier, it is desirable to have a (Write LARGE or SMALL) input resistance and a (Write LARGE or SMALL) output resistance.

   (vii) Depletion MOSFET can be also used as Enhancement MOSFET. Is it True or False?

   (viii) State the Barkhausen criterion for sustained oscillations in case of oscillator circuit using solid state amplifier.

   (ix) What is full form of CMRR and its ideal value in case of an Operational Amplifier?

   (x) What is Miller capacitance?

[Turn over

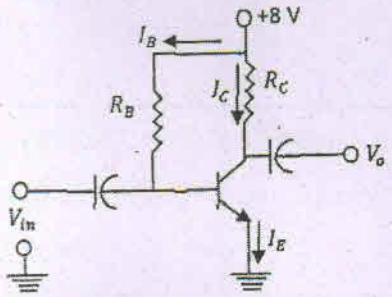
2. (a) Draw the circuit diagram of full-wave bridge rectifier and explain its operation. (5)

(b) Draw and explain the circuit diagram of a voltage doubler. (5)

(c) Explain the principle of working and application of varactor diode with necessary diagrams. (5)

3. (a) Draw and design a Zener voltage regulator circuit to provide output of 12 V for a maximum load current of 0.5 A when input voltage variation is 15 V to 18 V. (4)

(b) The transistor in the following figure has values of $h_{FE} = 100$. Determine the Q-point values of I_C and V_{CE}. (3 + 3 = 6)



(c) Draw a neat sketch of a single stage CE amplifer circuit using a Si PNP BJT having $\beta = 100$, potential divider bias resistances $R_1 = 20\text{k}$ and $R_2 = 2\text{k}$, Collector resistance $R_C = 1\text{k}$, Emitter resistance $R_E = 1\text{k}$ by passed by a capacitor, Load Resistance $R_L = 1\text{k}$ coupled to collector through a capacitor, Collector d.c. supply voltage $V_{CC} = 12V$ and a source voltage $V_s = 1mV$ with internal resistance $R_S = 1\text{k}$ connected to base through a coupling capacitor. Find current gain of the circuit. [Use r_E – parameter model of BJT]. (5)

4. (a) What is Early effect? Discuss its effects in a BJT. (5)

(b) For the operation of N-channel E-MOSFET it is necessary that gate voltage is highly negative. Is it True or False? Explain in brief with necessary figure. (5)

(c) Discuss in details about fabrication and operation of a depletion type N-channel MOSFET with necessary diagrams. (5)

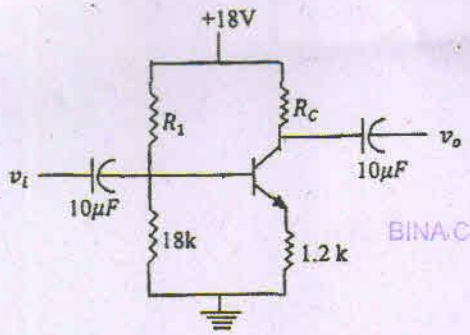
5. (a) Determine the feedback gain for an amplifier with negative feedback, having an output 30 V, for an input of 1.5 V. Consider that in absence of feedback, the same output is obtained for an input of 0.35 V. (3)

(b) Show that input resistance of a Voltage amplifier increases after Voltage-series feedback. (6)

(c) Discuss in details about the operation of crystal oscillator. (6)

6. (a) Draw the necessary circuit diagram and explain the use of Thermistor in base circuit as a bias compensator in case of biasing a CE configuration BJT. (5)

(b) Determine the values of R_1 and R_C for the network shown. Given that $\beta = 100$, $I_{CQ} = 2mA$ and $V_{CEQ} = 10V$. (5)



(c) Sketch the circuit for the electronic simulation of the differential equation given below. (5)

$$2\frac{d^2y}{dt^2} + 16\frac{dy}{dt} + 12\ y = g(t)$$

with initial conditions $y(0) = 12\ V$ and $y(0) = 12\ V$.

7. (a) Explain the procedures of measurement of input offset voltage and input bias current of an Operational Amplifier with necessary circuit diagrams and mathematical deductions. (3 + 3 = 6)

(b) Draw the circuit diagram of a triangular wave generator having inverting-input of a square wave generator shorted to ground and illustrate the operation of the circuit. Deduce the expressions of peak-to-peak output amplitude of the triangular wave and its time-period. (2 + 3 = 5)

(c) Explain the operation of a dual-input, balanced-output differential amplifier with constant current bias, with necessary circuit diagrams. (4)