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CS 131404

Roll No. of candidate

2019

B.Tech. 4th Semester End-Term Examination

COMPUTER ORGANIZATION AND ARCHITECTURE

(New Regulation)

(w.e.f 2017-2018)

Full Marks – 70 Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer Question No. 1 and any *four* from the rest.

1. Answer the following questions : (10 × 1 = 10)

(i) The decoded instruction is stored in ————

(a) IR (b) PC

(c) Registers (d) MDR

(ii) Which registers can interact with the secondary storage?

(a) MAR (b) PC

(c) IR (d) R0

(iii) The main virtue for using single bus structure is ————————

(a) Fast data transfers

(b) Cost effective connectivity and speed

(c) Cost effective connectivity and ease of attaching peripheral devices

(d) None of the mentioned

(iv) The instruction, Add #45,R1 does ————————

(a) Adds the value of 45 to the address of R1 and stores 45 in that address

(b) Adds 45 to the value of R1 and stores it in R1

(c) Finds the memory location 45 and adds that content to that of R1

(d) None of the mentioned

(v) Which representation is most efficient to perform arithmetic operations on the numbers?

(a) Sign-magnitude

(b) 1's complement

(c) 2's complement

(d) None of the mentioned

(vi) For the addition of large integers, most of the systems make use of ————————

(a) Fast adders

(b) Full adders

(c) Carry look-ahead adders

(d) None of the mentioned

(vii) The DMA transfers are performed by a control circuit called as

(a) Device interface

(b) DMA controller

(c) Data controller

(d) Over looker

(viii) The reason for the implementation of the cache memory is ————————

(a) To increase the internal memory of the system

(b) The difference in speeds of operation of the processor and memory

(c) To reduce the memory access and cycle time

(d) All of the mentioned

(ix) The computer architecture aimed at reducing the time of execution of instructions is _____

(a) CISC (b) RISC

(c) ISA (d) ANNA

(x) To increase the speed of memory access in pipelining, we make use of _____

(a) Special memory locations

(b) Special purpose registers

(c) Cache

(d) Buffers

2. (a) Distinguish between RISC and CISC architecture. (5)

(b) Explain with suitable diagram about the basic organization of a computer related to execution of a program. (5)

(c) Compare various bus organization techniques. (5)

3. (a) Explain base addressing and indexed addressing modes with an example. (5)

(b) Write an assembly language program to add two 8 bit numbers stored at address 2050 and address 2051. (5)

(c) Describe the register organization of a CPU. Use suitable diagram. (5)

4. (a) Compute (–9) + (–6) using 2's complement arithmetic. (5)

(b) Difference between static and dynamic RAM. (5)

(c) Assume that for a certain processor, a read request takes 50ns on a cache miss and 5ns on a cache hit. Suppose, while running a program, it was observed that 80% of the processors read requests result in a cache hit. What will be the average read access time in nanosecond? (5)

5. (a) Represent $(4.675)_{10}$ in IEEE 754 format. (Both single and double precision). (5)

(b) Design ALU and data path for STORE and JUMP instruction. (10)

6. (a) Solve –(5) * (–6) using Booth's multiplication algorithm. (5)

(b) How data hazards and control hazards can be handled? (5)

(c) A computer has 170 different operations. Word size is 4 bytes, one word instructions requires two address fields. One address for register and one address for memory. If there are 37 registers then what is the memory size is in KB? (5)

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