03-07-19

Total No. of printed pages = 4

**EC 131407**



Roll No. of candidate

**2019**

**B.Tech. 4th Semester End-Term Examination**

**INTRODUCTION TO DIGITAL ELECTRONICS**

**(New Regulation)**

**(w.e.f. 2017-18)**

Full Marks – 70 Time – Three hours

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The figures in the margin indicate full marks for the questions.

Answer question No. 1 and any *four* from the rest.

1. Answer the following : (10 × 1 = 10)

   (a) What do you understand by the term 'digital'?

   (b) What do you mean by logic design?

   (c) 0111 is an excess-3 of ——————?

   (d) Realize the logical expression $Y = \overline{A \oplus B}$ and name the gate.

   (e) Find the decimal equivalent of the binary number (1111) assuming sign magnitude representation of binary number.

   (f) Represent $(-17)_{10}$ in 2's complement form.

   (g) What is the BCD equivalent of 57?

[Turn over

(h) ———— is the fastest logic family.

(i) ———— is a binary cell capable of storing one bit Information.

(j) Define the term 'fan-out'.

2. (a) Convert $(101101.10101)_2 = (\quad)_{10}$ $(5 \times 3 = 15)$

(b) Convert $(10.625)_{10} = (\quad)_2$

(c) Convert $(675.625)_{10} = (\quad)_{16}$

(d) Convert $(A72E)_{16} = (\quad)_8 = (\quad)_2$

(e) Convert $(3287.5100098)_{10} = (\quad)_8$.

3. (a) Convert the following Boolean function into standard POS and express it in terms of maxterm. $(5 \times 3 = 15)$

$Y(A, B, C) = (A + B)\ (B + \overline{C})\ (A + C)$

(b) Prove De-Morgan's Theorems.

(c) Minimize :

$$y = \overline{\overline{x\overline{y} + xyz + x(y + x\overline{y})}}$$

(d) Perform using 2's complement method (use 8-bit representation) : 48-23

(e) Perform $(26)_8 - (75)_8$.

4. (a) Simplify using Quine-McCluskey method. $(10 + 5 = 15)$

$$Y(A, B, C, D) = \sum m(1, 2, 3, 5, 9, 12, 14, 15) + d(4, 8, 11)$$

(b) Minimize using K-map :

$$f(A, B, C, D) = \sum m(1, 5, 7, 8, 9, 10, 11, 14, 15) + d(2, 12, 13)$$

5. (a) Draw the full-adder circuit using two half-adders. Also realize the circuit using only NAND gates. (2+3=5)

(b) Implement the following logic function using 4:1 MUX (4)

$$F(A, B, C) = \sum m(1, 2, 4, 7)$$

(c) Design a parity general or to produce digital word with even parity. Assume the inputs to be three bit binary word. (3)

(d) What is a magnitude comparator? Describe a logic diagram for a 1-bit magnitude comparator. (3)

6. (a) Name some applications of counter. (2)

(b) What is a universal shift register? (2)

(c) Define the terms : (2)

(i) propagation delay

(ii) figure of merit.



(d) For an S-R flip-flop, what will be output if input changes from : (2)

(i) $S = 1, R = 0$ to $S = R = 0$

(ii) $S = 0, R = 1$ to $S = R = 0$

(e) Explain the terms : Modulus of a counter, Down-counter. (2)

(f) (i) What is a flip-flop? (5)

(ii) Why $S = R = 1$ is not permitted in the S-R flip-flop?

(iii) What is race-around condition in J-K flip-flop?

(iv) Explain the operation of Master-slave J-K flip-flop.

7. (a) What are the different modes of operation of shift register? Explain the operation of a register in PIPO mode. (5)

(b) Compare the performance of TTL, CMOS and ECL logic. (5)

(c) Write short notes on (any *one*) : (5)

(i) programmable logic array

(ii) binary codes.