Total No. of printed pages = 3

ECE 1816 PE 11

Roll No. of candidate

2022

B.Tech. 6th Semester End-Term Examination

DIGITAL SYSTEM DESIGN USING VERILOG

(Odd Semester)

(New Regulation and New Syllabus)

Full Marks – 70

Time – Three hours

The figures in the margin indicate full marks for the questions.

GROUP – A

1. Answer all the questions : (10 × 1 = 10)

(i) Delays can be introduced in a circuit, with a

(a) Buffer (b) EXOR gate

(c) Inverter (d) Flip-flops

(ii) The VErilog HDL code starts with the keywords

(a) Always (b) Module

(c) Endmodules (d) Items

(iii) The meaning of RTL is

(a) Resistor-transfer logic (b) Register-transfer logic

(c) Resistor-transistor logic (d) Register transistor logic

(iv) A decoder with input 4, will have

(a) 15 numbers of output (b) 8 numbers of output

(c) 16 numbers of output (d) None

(v) A Latch has

(a) One stable state (b) Two stable state

(c) Three stable state (d) Infinite stable state

[Turn over

(vi) The symbol used for bitwise AND operation is

(a) And (b) AND

(c) $ (d) &

(vii) The default value for reg data type

(a) 0 (b) 1

(c) Z (d) X

(viii) Operators which precedes the operand is

(a) Unary (b) Binary

(c) Ternary (d) None

(ix) To trigger an event the operator to be used is

(a) ---> (b) =>

(c) @ (d) ==

(x) Testbench is

(a) Generate stimulus and apply to DUT

(b) Capture response and check for correctness

(c) Measure progress against verification goals

(d) All of the above.

GROUP – B

Answer any four questions

2. (a) Explain the levels for design description in Verilog HDL. (8)

(b) Explain in detail about the DATA types in Verilog HDL. (7)

3. (a) Write Verilog HDL source code for a gate level description of 4 to 1 multiplexer circuit. Draw the relevant logic diagram. (7)

(b) Explain the following constraints: (4)

(i) Noise margin

(ii) Propagation delay

(c) State the differences between TASK and FUNCTIONS. (4)

4. (a) What are the timing controls associated with behavioral model. (5)

(b) Define functional Bifurcation. Explain about forever loop. (5)

(c) Write the Verilog code for an 8 bit register with a synchronous reset input and a tri- state output controlled. (5)

5. (a) What do you mean by User Defined Primitives (UDP) and explain the types with examples? (4)

(b) Write the Verilog code for half subtractor using CMOS switches. (5)

(c) Define overriding parameters. (2)

(d) Describe Procedural and Conditional Assignments. (4)

6. (a) What are the types of sequential models? (5)

(b) What are the various sequential memory storage models? Explain in detail about each of them. (8)

(c) Define state machine coding. (2)

7. (a) Explain test bench techniques. How the simulation of test bench can be controlled? Explain with help of an example. (9)

(b) Write a brief short note on Path Delays and Simulation. (6)