Total No. of printed pages = 3

ECE 1818 PE 31

23/6/22

Roll No. of candidate | | | | | | | | | | |

BINA CHOWDHURY CENTRAL LIBRARY
(GIMT & GIPS)
Azara, Hatkhowapara,
Guwahati -781017

2022

B.Tech. 8th Semester End-Term Examination

MIXED SIGNAL DESIGN

(ECE + ETE)

(New Regulation 2017-18) &

(New Syllabus 2018-19)

Full Marks – 70 Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer question No. 1 and any *four* from the rest.

1. Answer the following (MCQ/ Fill in the blanks) : (10 × 1 = 10)

(i) According to the principle of current mirror if gate-source potentials of two identical MOS transistors are equal, then the channel currents should be _____

(a) Equal
(b) Different
(c) Both (a) and (b)
(d) None of the above

(ii) In two-stage op-amp, what is the purpose of compensation circuitry?

(a) To provide high gain
(b) To lower output resistance and maintain large signal swing
(c) To establish proper operating point for each transistor in its quiescent state
(d) To achieve stable dosed-loop performance

(iii) An ideal op-amp has _____

(a) Infinite input resistance
(b) Infinite differential voltage gain
(c) Zero output resistance
(d) All of the above

[Turn over

(iv) The cascade amplifier is a multistage configuration of

(a) CC-CB (b) CE-CB

(c) CB-CC (d) CE-CC

(v) A differential amplifier is invariably used in the i/p stage of all OP-Amps. This is done basically to provide the OP-Amps with a very high

(a) CMRR (b) Bandwidth

(c) Slew rate (d) Open-loop gain

(vi) The effective channel length of a MOSFET in saturation, decreases with increase

(a) Gate voltage (b) Drain voltage

(c) Source voltage (d) Body voltage

(vii) Which of the following is not an advantage of under sampling?

(a) slower ADC (b) less power

(c) fast microprocessors (d) less memory capacity

(viii) Which of the following is the fastest ADC

(a) Successive approximation

(b) Delta encoded conversion

(c) Flash conversion

(d) Pipelined conversion

(ix) At which state the phase-locked loop tracks any change in input frequency?

(a) Free running state

(b) Capture State

(c) Phase locked state

(d) All of the mentioned

BINA CHOWDHURY CENTRAL LIBRARY
(GIMT & GIPS)
Azara, Hatkhowapara,
Guwahati -781017

(x) What is the function of low pass filter in phase-locked loop?

(a) Improves low frequency noise

(b) Removes high frequency noise

(c) Tracks the voltage changes

(d) Changes the input frequency

2. (a) What is switched capacitor? What is its significance in the CMOS technology? (2 + 3 = 5)

(b) If $C1 = C2 = C$, find the value of C that will emulate a 1 mΩ resistor if the clock Frequency is 200 KHz. (5)

(c) Draw and describe the switched capacitor filter circuit. (5)

3. (a) Derive the voltage gain and output impedance of source follower. (8)

(b) Draw and explain folded cascode configuration and list out its advantages. (7)

4. (a) Explain the working and derive the output impedance of a simple MOS current mirror. (8)

(b) Derive the output impedance of differential amplifier with MOS current source Load. (7)

5. (a) What is a flash converter? Explain the function of a 3 bit flash ADC. (7)

(b) What is time interleaving? Explain the operation of a time interleaved ADC. (8)

6. (a) Explain about the basic charge pump PLL with a neat figure. (7)

(b) With the help of necessary waveforms, explain about the non-ideal effects in PLLs. (8)

7. (a) With neat circuit diagram, explain two stage open loop comparator circuit. (7)

(b) Write short notes on (i) Pipeline ADCs (ii) High speed comparator. (4+4 =8)

BINA CHOWDHURY CENTRAL LIBRARY
(GIMT & GIPS)
Azara, Hatkhowapara,
Guwahati -781017