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EC 1318 E 042

Roll No. of candidate | | | | | | | | | | |

2019

B.Tech. 8th Semester End-Term Examination

ECE

CAD FOR VLSI (ELECTIVE – IV) Departmental

Full Marks – 100 Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer question No. 1 and any *six* from the rest.

1. Answer the following : (10 × 1 = 10)

   (i) The specification of a system is a compromise between ————————.

   (ii) What is the complexity of DFS ————————.

   (iii) Since layout data is typically sent to fabrication on a tape, the event of release of data is called ————————.

   (iv) ———————— law still valid to determine technology roadmap for electronic devices.

[Turn over

(v) Digital Signal Processing (DSP) architectures have been successfully synthesized by _____.

(vi) The extracted description is compared with the circuit description to verily its correctness. This process is called _____.

(vii) _____ routing is a term used to describe routing over blocks and active areas.

(viii) Empty space between cells in a row is called a _____.

(ix) The data structure used in standard implementation of Breadth First Search is _____.

(x) _____ is a process which verifies that all geometric patterns meet the design rules imposed by the fabrication process.

2. (a) What are the advantages associated with Silicon on Insulator and Silicon Germanium process innovation? (5)

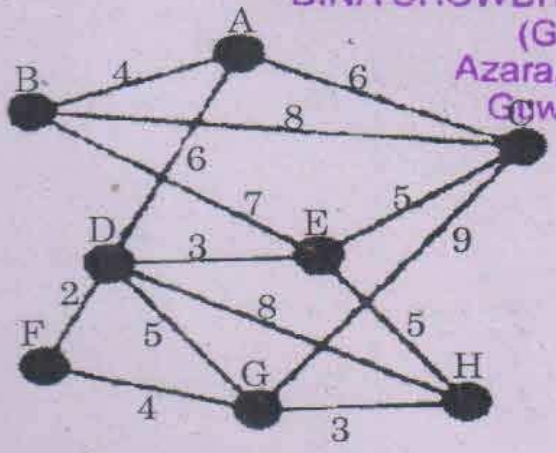
(b) State and explain the issues related to fabrication process. (10)

3. (a) Why physical design starts very early in the design cycle? (5)

(b) Discuss VLSI physical design cycle. (10)

4. (a) Discuss with suitable diagram class NP and Class P problem. (5)

(b) Explain Djikstra's algorithm and Find shortest path between B and G (10)



5. (a) Explain the factors that are considered by the chip planning. (7)

(b) Discuss constraints and objectives of the partitioning process. (8)

6. (a) What are the designs style specific placement problems? (7)

(b) Write algorithm for DFS and explain with suitable example. (8)

7. (a) Explain simulated annealing with proper algorithm. (10)

(b) Explain why present VLSI circuits use MOSFETS instead of BJTs? (5)

8. (a) Compare global routing and detailed routing. (4)

(b) Why we need to have CAD tools for VLSI design? Name some CAD tools used for VLSI Design. (5)

(c) Explain with suitable example "Kruskal's" Algorithm. (6)

9. (a) What are the difference between synthesis and simulation? (5)

(b) Discuss different features of FPGA. (5)

(c) Explain the role of compaction in VLSI design. (5)
