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EC 131802

Roll No. of candidate

2019

B.Tech. 8th Semester End-Term Examination

COMPUTER ARCHITECTURE AND ORGANIZATION

Full Marks – 100 Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer question No. 1 and any *six* from the rest.

1. Multiple choice question: (10 × 1 = 10)

(i) The circuit used to store one bit of data is known as

(a) Register
(b) Encoder
(c) Decoder
(d) Flip

(ii) The ALU makes use of ———— to stone the intermediate results

(a) Accumulator
(b) Registers
(c) Stack
(d) None of the above

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(iii) ———— are numbers and encoded characters, generally used as operands

(a) Input

(b) Data

(c) Information

(d) Stored values

(iv) The main virtue for using single bus structure is

(a) Fast data transfer

(b) Cost effective connectivity

(c) Cost effectivity connectivity and ease of attaching peripheral device

(d) None of the above

(v) Only ———— is connected to the address i/p of memory

(a) Program counter

(b) Stack pointer

(c) Address register

(d) Data register

(vi) Which method/s of representation of numbers occupies a large amount of memory than others

(a) Sign–Magnitude

(b) 1's complement

(c) 2's complement

(d) None of the above

(vii) Which method of representation has two representation for "0"

(a) Sign–Magnitude

(b) 1's complement

(c) 2's complement

(d) None of the above

(viii) The registers used to store the flags is called as

(a) Flag register

(b) Status register

(c) Test register

(d) Log register

(ix) In a normal n-bit adder to find out if an overflow has occurred, we make use of

(a) AND gate

(b) NAND gate

(c) X-OR gate

(d) NOR gate

(x) ———— bus structure is usually used to connect I/O devices

(a) Single

(b) Multiple

(c) Star

(d) All the above

2. (a) Given the Boolean expression F=X'Y+XYZ' (2+2+3=7)

(i) Derive an algebric expression for F'

(ii) Show that F.F'=0

(iii) Show that F+F'=1

(b) A sequential circuit has two D f/f 'A' and 'B', two i/p 'x' and 'y' and one o/p' z'. The f/f equations and circuit o/p are as follows (5+3=8)

$$D_A=x'y+xA$$

$$D_B= x'B+xA$$

$$Z=B$$

(i) Draw the logic diagram of the circuit

(ii) Tabulate the state table

3. (a) How negative numbers are represented in computer? Explain with example. (4)

(b) Represent $(-0.825)_{10}$ in IEEE 754 floating point representation. (4)

(c) Draw the logic diagram of a 2 to 4 line decoder with only NOR gate. Include an enable i/p (4)

(d) How many numbers of bytes that can be stored in the memories

(i) 2K*16

(ii) 64K*8

(iii) 16M*32 (3)

4. (a) How a common bus system can be achieved with a 3 state buffer? Explain with a diagram. (5)

(b) Design a 4 bit combinational circuit decrementer using 4 full adder circuits. (5)

(c) Design a digital circuit that performs the four logic operations of Ex-OR, Ex-NOR, NOR and NAND. (5)

5. (a) What are the difference between direct and indirect addressing? Explain with a suitable diagram. (5)

(b) What are the differences between hardwired control and micro-programmed control? Explain the micro-programmed control unit with a suitable diagram. (7)

(c) Consider the following micro-operation: AR←PC. Write the steps of instruction that is to be required for execution of this micro operation that uses a common bus. (3)

6. (a) Draw and explain the flow chart for Booth's algorithm for its complement multiplication. (5)

(b) Using Booth's algorithm show the multiplication $(-3)_{10}*(-7)_{10}$. (8)

(c) Convert the following number into equivalent binary number: (2)

(i) $(1975)_{10}$

(ii) $(F89)_{16}$.

7. (a) What are static and dynamic RAM? (2)

(b) Using a block diagram, explain how virtual address is translated into a physical address in a computer which uses virtual memory. (8)

(c) The access time of a cache memory is 100 nsec and that of main memory is 1000 nsec. It is estimated that 80 percent of the memory request are for read and the remaining 20 percent for write. The hit ratio for read access only is 0.9. A write through procedure is used. What is the average access time of the system considering only memory read cycles? (5)

8. (a) Draw space time diagram of a four segment pipeline showing the time it takes to process 8 tasks. (5)

(b) Formulate a six-segment instruction pipeline for a computer. Specify the operations to be performed in each segment. (5)

(c) The time delay of the 4 segments in the pipeline are as follows: t_1=50 nsec, t_2=30 nsec, t_3=95 t_4=45 nsec. The interface registers delay time t_r=5 nsec. How long would it take to add 100 pairs of number in the pipeline. (5)

9. Write short notes on (any three): (3 × 5=15)

(a) Different generations of computer

(b) Basic structure of a computer

(c) Interrupt Cycle

(d) Associated memory