Total No. of printed pages = 4

EC 1318E042

Roll No. of candidate | | | | | | | | | | |

2020

B.Tech. 8th Semester End-Term Examination

ECE

CAD FOR VLSI (ELECTIVE IV)

Full Marks – 50 Time – Two hours

The figures in the margin indicate full marks for the questions.

Answer Question No. 1 (any *five*) and any 3 (*three)* from the rest.

1. Answer the following : $(5 \times 1 = 5)$

   (i) Lowest level of power consumption occurs in _____.

   (ii) What is the complexity of BFS?

   (iii) In FPGA, the connection between a horizontal segment and a vertical segment is provided through a _____.

   (iv) _____ law still valid to determine technology roadmap for electronic devices.

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(v) When pins are brought to the top of the block as a sea-of-pins. It is called _____.

(vi) Geometric information is extracted to compute Resistance and Capacitance. The extracted information is also used to check the reliability aspects of the layout. This process is called _____.

(vii) _____ and _____ technique is used to removes troublesome connections and reroutes them in a different order.

(viii) Cells are placed in rows and the space between two rows is called a _____.

(ix) The data structure used in standard implementation of Depth First Search is _____.

(x) _____ is a process which verifies that all geometric patterns meet the design rules imposed by the fabrication process.

2. (a) State Moore's law, and explain its applicability to current scenario? (5)

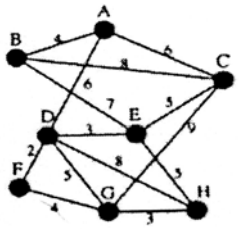
(b) State and explain the issues related to fabrication process? (10)

3. (a) What are the most common type of placement problems ? (5)

(b) Discuss VLSI design cycle. (10)

4. (a) What are the algorithms for NP Hard problem? (5)

(b) Explain Prim's algorithm and Find shortest path between B and G. (10)



5. (a) What are the ways of checking correctness of an IC without actually fabricating it? (7)

(b) Why partitioning is required? What are the types of partitioning? Explain. (8)

6. (a) Why improper floor planning lead to unroutable designs? How we can address the issue. Explain. (7)

(b) Write algorithm for topological search and explain with suitable example. (8)

7. (a) Explain simulated annealing with proper algorithm. (10)

(b) State and explain different levels of simulation? (5)

8. (a) Compare global routing and detailed routing. (5)

(b) Why we need to have CAD tools for VLSI design? Name some CAD tools used for VLSI Design. (5)

(c) Write a short note on common design styles used in VLSI Design cycle. (5)

9. (a) What are the difference between synthesis and simulation? (5)

(b) Write VHDL code for full adder with an objective of less area utilization by full adder. Draw its graph. (10)

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