Total No. of printed pages = 6

EC 131802

Roll No. of candidate | | | | | | | | | | |

2020

B.Tech. 8th Semester End-Term Examination

ECE

COMPUTER ARCHITECTURE AND ORGANIZATION

Full Marks – 50 Time – Two hours

The figures in the margin indicate full marks for the questions.

Answer Question No. 1 (any *five*) and any 3 (*three*) from the rest.

1. Answer the following (MCQ) : $(5 \times 1 = 5)$

   (i) The small extremely fast, RAM's are called as _____.

   (a) Cache (b) Heaps

   (c) Accumulators (d) Stacks

   (ii) _____ is used to store data in registers.

   (a) D flip flop

   (b) JK flip flop

   (c) RS flip flop

   (d) None of the mentioned

[Turn over

(iii) The main virtue for using single Bus structure is

(a) Fast data transfers

(b) Cost effective connectivity and speed

(c) Cost effective connectivity and ease of attaching peripheral devices

(d) None of the mentioned

(iv) Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster?

(a) A

(b) B

(c) Both take the same time

(d) Insufficient information

(v) In the case of, Zero-address instruction method the operands are stored in

(a) Registers

(b) Accumulators

(c) Push down stack

(d) Cache

(vi) When we use auto increment or auto decrements, which of the following is/are true?

(1) In both, the address is used to retrieve the operand and then the address gets altered

(2) In auto increment, the operand is retrieved first and then the address altered

(3) Both of them can be used on general purpose registers as well as memory locations

(a) 1, 2, 3 (b) 2

(c) 1, 3 (d) 2, 3

(vii) If a system is 64 bit machine, then the length of each word will be _____.

(a) 4 bytes (b) 8 bytes

(c) 16 bytes (d) 12 bytes

(viii) The return address from the interrupt-service routine is stored on the _____.

(a) System heap (b) Processor register

(c) Processor stack (d) Memory

(ix) To resolve the clash over the access of the system BUS we use _____.

(a) Multiple BUS

(b) BUS arbitrator

(c) Priority access

(d) None of the mentioned

(x) The advantage of CMOS SRAM over the transistor one's is _____.

(a) Low cost

(b) High efficiency

(c) High durability

(d) Low power consumption

2. (a) Draw a 3-8 decoder using 2-4 decoders. (3)

(b) Draw and explain one bit arithmetic logic shift unit. (5)

(c) Draw and explain a 4-bit synchronous binary counter. (7)

3. (a) Find the (r-1)'s and r's complement of the following decimal and binary numbers. (5)

(i) 546700

(ii) 1011001.

(b) With examples show how negative number are represented in computers? (3)

(c) With the help of a diagram explain the common bus system of a basic computer. (7)

4. (a) Draw the flowchart for instruction cycle of a basic computer. (5)

(b) Explain the microprogrammed control organization. (6)

(c) Explain the Polish notation and Reverse Polish notation with an example. (4)

5. (a) Explain the various types of addressing modes with examples. (8)

(b) Differentiate between RISC and CISC computers. (7)

6. (a) Draw and explain the pipelining for floating point addition and subtraction. (7)

(b) Explain in details what is vector processing and array processing. (8)

7. (a) With relevant diagrams explain addition and subtraction of signed magnitude data. (7)

(b) Explain the Booths algorithm for multiplication of 2's complement numbers. (8)

8. (a) A hierarchical cache main memory sub system has the following specifications:

Cache access time of 50 ns

Main memory access time of 500 ns

80% of memory request are for read operation

Hit ratio of 0.9 for read access and a write through mechanism.

Calculate the following :

(i) Average access time of memory system considering only read cycle.

(ii) Average access time of system for both read and write request. (8)

(b) What is page replacement policy for cache memory? Describe two page replacement policies for cache memory. (7)

9. Write short notes on (any *three*) : $(3 \times 5 = 15)$

(a) Hardwired control unit.

(b) Pipelining

(c) DMA

(d) Computer Generations.

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