Total No. of printed pages = 3

ECE 1816 PE 11

19/6/23

Roll No. of candidate | | | | | | | | | | |

2023

B.Tech. 6th Semester End-Term Examination

DIGITAL SYSTEM DESIGN USING VERILOG

(New Regulation (w.e.f 2017 – 18) & New Syllabus (w.e.f. 2018 – 19))

Full Marks – 70 Time – Three hours

The figure in the margin indicate full marks for the questions.

GROUP – A

1. Answer *all* the questions :

(i) The digital logic family which has minimum power dissipation is

(a) TTL (b) RTL

(c) DTL (d) CMOS

(ii) Verilog supports ———— but not VHDL

(a) Behavioral level (b) Dataflow level

(c) Gate level (d) Switch level

(iii) The wait statement in Verilog is

(a) Level sensitive (b) Edge sensitive

(c) Both (d) None

(iv) A 6 states FSM requires minimum

(a) 2 – bit states (b) 3 – bit states

(c) 4 – bit states (d) None of the above

(v) Compared to the carry-look ahead adder, the ripple-carry adder is:

(a) Slower and Smaller (b) Slower and Bigger

(c) Smaller and Faster (d) Bigger and Faster

(vi) Case statements produces

(a) Serial logic (b) Parallel logic

(c) Priority encoded logic (d) Priority decoded logic

[Turn over

(vii) Inertial delay is defined as

(a) The time that it takes for a gate to change its output

(b) Delay caused by the wires resistance

(c) Propagation delay

(d) Delay caused by the wire capacitance

(viii) The sensitivity list indicates

(a) When a change occurs to any one of elements in the list, the block of statements inside begin...end will get executed.

(b) When a change occurs to any one of elements in the list, the block of statements inside begin.., end will get executed only when all the elements in the list changes

(c) The statements associated with the elements of the list gets executed

(d) When any change occurs to any statement before begin, the inside statements of begin....end will get executed.

(ix) How many data select lines are required for selecting eight inputs in a mux?

(a) 1 (b) 2

(c) 3 (d) 0

(x) Instance created when

(a) A Module is written using Verilog HDL

(b) When stimulus block is written using Verilog HDL

(c) When a module is invoked in another module using an instance id

(d) None of the above

GROUP – B

Answer any *four* questions

2. (a) List the importance of HDL. (3)

(b) Discuss the different levels of abstraction used in Verilog modelling. (6)

(c) Explain the following data types with example in verilog. (6)

(i) Nets

(ii) Register

(iii) Vectors

3. (a) Write Verilog HDL module of SR latch (5)

(b) Differentiate between task and functions. (4)

(c) What are the basic components of module? Explain them with reference to verilog. (6)

4. (a) Explain Carry Look Ahead adder. Write a Verilog code with data flow style program for carry look ahead adder. (6)

(b) Explain with an example how 'while' construct is used. (4)

(c) How delays are introduced in verilog programming? Why these are needed? (5)

5. (a) Design a 3 to 8 bit decoder (5)

(b) Write down the Verilog code that defines the UDP which performs the following Boolean function (6)

$F(a,b,c) = \Sigma(0, 2,4,6,7)$

(c) Compare blocking and non-blocking assignments. (4)

6. (a) Write short notes on (6)

(i) Logical Operators

(ii) Conditional Operators

(iii) Arithmatic Operators

(b) Write in detail about assertion verification and also give its benefits. (6)

(c) Define synthesis and simulation. (3)

7. (a) What is the distinction between a Moore and Mealy finite state machine? (2)

(b) What is test bench? Implement NAND gate using MOS switches and test it with suitable test-bench. (7)

(c) Explain capacitive model of a sequential circuit and compare it with other models. (6)
