Total No. of printed pages = 3

ECE 181402

Roll No. of candidate

2023

B.Tech. 4th Semester End-Term Examination

ANALOG CIRCUITS

New Regulation (w.e.f. 2017-18) & New Syllabus (w.e.f. 2018-19)

Full Marks – 70   Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer question No. 1 and any *four* from the rest.

1. Answer the following (MCQ/ Fill in the blanks) :   (10 × 1 = 10)

    (i)   The speed of op amp circuits is limited by the ——————— of the opamps

    (ii) Compared with single – ended signals, differential signals are ———————
          immune to common-mode noise

    (iii) In a sample and hold circuit ——————— amplifier is used

          (a) a unity gain non inverting amplifier

          (b) a unity gain inverting amplifier

          (c) an inverting amplifier with a gain of 10

          (d) an inverting amplifier with a gain of 100

    (iv) Voltage series feedback results in

          (a) increase in both input and output impedance

          (b) decrease is both input and output impedance

          (c) increase in input and decrease in output impedance

          (d) decrease in input and increase in output impedance

    (v)   Power amplifier amplifies

          (a) only voltage of a signal   (b) only current of a signal

          (c) only power of a signal   (d) all of the above

[Turn over

(vi) The magnitude of the loop gain must exceed —————— at the oscillation frequency. This is called the "startup condition".

(vii) To avoid oscillation, the gain cross over frequency must fall —————— the phase cross over frequency

(viii) Which of the following has poorest linear performance

    (a)   Class A   (b)   Class B

    (c)   Class C   (d)   Class AB

(ix) Primary trigger for Oscillation is obtained from

    (a)   DC voltage   (b)   Noise voltage

    (c)   External trigger   (d)   No triggering

(x) The condition of keep BJT in active mode is ——————

2. (a) The CE topology is biased with a collector current of 1mA and $R_c = 1\,k\Omega$. If $\beta = 100$ and $V_A = 10V$, determine the small – signal voltage gain and the I/O impedance. (5)

(b) Design the stage of Fig. 1 to satisfy the following conditions : $I_C = 1mA$, voltage drop across $R_E = 400\,mV$, voltage gain = 20 in the audio frequency range (20 Hz to 20 kHz), input impedance $> 2k\Omega$. Assume $\beta = 100$, $I_s = 5 \times 10^{-16}$, and $V_{cc} = 2.5V$. (7)
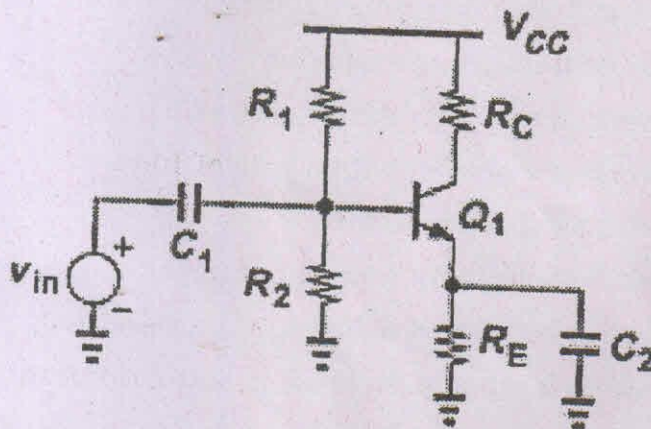
(c) What is cross over distortion? (3)

Fig. 1

3. (a) Derive the small signal gain, input, and output impedance of Emitter Follower. (10)

(b) Explain the working of Current Mirror using suitable diagram. (5)

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4. (a) Explain the working of the Cascode Amplifiers and derive its different parameters.

(b) Compare Class A, B, AB and C amplifiers.

(c) What are the effect of coupling and by pass capacitor?

5. (a) Design a non inverting amplifier for the following specification: closed – loop gain = 5, gain error = 1% closed –loop bandwidth = 50 MHz. Determine the required open-loop gain and bandwidth of the op amp. Assume the op amp has an input bias current of $0.2 \ \mu A$. (5)

(b) Design an integrator for a unity-gain frequency of 10 MHz and an input impedance of $20 \ k\Omega$. If the op amp provides a slow rate of 0.1 V/ns, what is the largest peak-to-peak sinusoidal swing at the input at 1 MHz that produces an output free from slewing? (5)

(c) Mention the characteristics of an ideal op amp. (5)

6. (a) Explain the basic structure and principle of operation of differential amplifier. Derive differential gain, common mode gain, CMRR and ICMR for the same.

(b) Discuss different types of RC Oscillators.

(c) Explain the working principle of a comparator.

7. Write a short note on (any *three*) : $(3 \times 5 = 15)$

(a) High Pass Filter

(b) Colpitts Oscillators

(c) Current Series feedback topology

(d) Sample and Hold Circuits

(e) RC coupled Amplifier.

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