M 058/033

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MCA Semester Examinations

COMPUTER ORGANIZATION AND ARCHITECTURE

Course Code: MCA23502T

Full Marks – 60 **Time –2 1/2 hours**

The figure in the margin indicates full marks for the questions.

Part A

Answer **ALL** questions

Multiple Choice (**10 x 1mark = 10marks**)

1. **a)** The 8-bit 2's complement form of the number -14 is _____

(i) 00001110 (ii) 11110010 (iii) 10001110 (iv) 01110001

b) Which of the following memory of the computer is used to speed up the computer processing?

(i) RAM (ii) ROM (iii) Hard disks (iv) Cache memory

c) CISC stands for –

(i) Complex Instruction Set Computer

(ii) Complete Instruction Sequential Compilation

(iii) Complex Instruction Sequential Compiler

(iv) None of the above

d) On adding the 1's complemented numbers 0011 and -1101, the result is

(i) -1010 (ii) 1011 (iii) -1000 (iv) 1100

e) JP instruction in 8085 architecture is set to 1 if the parity flag gives even parity.

(i) True (ii) False

f) On receiving an interrupt from an I/O, CPU

(i) halts for predetermined time

(ii) branches to interrupt service routine after completing current instruction

(iii) branches to interrupt service routine immediately

(iv) hands over the control of address bus and data bus to I/O

g) Multiprocessor refers to the existence of two or more programs indifferent parts of the memory at same time.

(i) True (ii) False

h) In Boolean algebra, what is (A**.**A**'**) + A ?
(i) 0 (ii) 1 (iii) A (iv) A**'**

i) Ina 16 x 1 multiplexer, there are 16 input lines, 5 select lines and 1 output line.
(i) True (ii) False

j) In bus system, address bus and control bus are
(i) unidirectional and bidirectional respectively
(ii) bidirectional and unidirectional respectively
(iii) unidirectional and unidirectional respectively
(iv) bidirectional and bidirectional respectively

Part B

Answer **ANY FOUR** questions (*Word limit for each answer is 50*)
(**4 x 5 mark = 20 marks**)

2. Given a binary string 110010100011**.**10110. Find the octal and hexadecimal equivalent of the given binary string.
3. Distinguish between isolated I/O and memory-mapped I/O.
4. Find the minimal SOP expression for the following Boolean function.
F(A, B, C, D) = ∑(0, 5, 6, 7, 8, 10, 11, 13, 14, 15)
Also, find the complement form of the minimal SOP.
5. Show the floating-point representation of $(-55.625)_{10}$ using 1 sign bit,6 exponent bits and 10 mantissa bits.
6. Discuss the basic operation of cache memory. Consider the number of cache hits to be 42 and the number of cache misses to be 5. Then, what is the hit ratio?
7. Find the binary equivalent of a number Q where Q is obtained as Q = (-5) * P and for P, its 2's complement representation is 11100101.

Part C

Answer **ANY TWO** questions (*Word limit for each answer is 50*)
(**2 x 10 mark = 20 marks**)

8. **a)** Apply Booth's method to find the binary multiplication of two binary numbers where the multiplicand is 0000 and the multiplier is 0110 in 2'scomplement representation. 5
b) Explain about SR flip flop with its circuit diagram and characteristic table and equation. 5

9. **a)** Illustrate about the different types of Flag registers used in 8085architecture. 4
b) Find the number of bits in Tag and Line number field for direct mapped cache of size 64 KB when the main memory size is 1024 KB with block size of 256 bytes. 6

10. **a)** What advantage handshaking asynchronous data transfer has over strobe control? Summarize about source-initiated handshaking method. 2+3=5
b) Define data transfer instructions? Discuss different data transfer instructions with examples from 8085 architecture. 2+3=5

Part D

Short Notes

(**2 x 5 mark = 10 marks**)

11. Write **ANY TWO**: (*Word limit for each answer is 70*)

a) Direct memory access mode of transfer.

b) Indirect addressing mode with its advantage and example.

c) Hardwired and Micro programmed control unit

d) Virtual memory address mapping using pages

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